IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 10, October 2016

Modified Vedic Multiplier using Koggstone Adders

Y. Rama Lakshmanna[1], G.V.S. Padma Rao[2], K. Bala Sindhuri[3], N. Udaya Kumar[4]

PG Student, SRKR Engg. College, Bhimavaram, India[1]

Professor, SRKR Engg College, Bhimavaram, India[2, 4]

Assistant Professor, SRKR Engg. College, Bhimavaram, India[3]

Abstract: Multipliers play the key role in the design of high speed arithmetic logic units, Internet of things and digital signal processing applications. Multipliers using Vedic mathematics with different adders improve the performance of the multiplier. Performance parameters like less gate count and high speed are obtained in Vedic multipliers by using different techniques like Carry select adder, Carry save adder and Binary to Excess-1 converter. Vedic multiplier using koggestone adder gives better performance in terms of area, when compared to Vedic multiplier using CSLA. The multiplier is implemented on Spartan 3E FPGA and simulation is performed using verilog HDL.

Keywords: Binary to Excess -1 converter (BEC), Carry save adder (CSA), Carry Select adder (CSLA), Koggstone adders (KSA), Vedic multiplier**.**

I. INTRODUCTION

Multipliers, adders, shift registers are key elements in digital processing and wireless communication. They are mostly used in image processing applications and it is essential in fields of mapping, holography, x-ray imaging, robotics and medical image processing[1].Array multiplier is the traditional method for multiplication, in which partial products are generated by means of AND gates. Adding of partial products is done by means of ripple carry adders, which is time consuming process. If the size of multiplier & multiplicand is very large, Array multiplier is not suitable, Since the propagation of carrier consumes more time while performing addition.[2] Speed can be achieved by means. In order to achieve more speed, addition is performed by means of carry save adder (CSA) instead of ripple carry adder [3]-[4].Power consumption is also high for an array multiplier. In order to improve the performance of the multiplier, booth multiplier is designed.

The performance parameters like speed, power consumption are improved by reducing the number of partial products. Signed multiplication and unsigned multiplication can be performed by using Booth multipliers. Speed can be achieved by using Radix-2, Radix-4 multiplier in Booth algorithm[5]-[6]. The performance is further improved by using udrhva tiryakbhyam of ancient Indian Vedic Mathematics by using ROM approach. Decimal and Binary multiplication is performed using Vedic mathematics for which area is very less when compared to array multiplier. Performance parameters such as speed, delay are improved by means of less computations[7].In order to improve speed addition of partial products is realized using carry skip technique which uses different sizes of adders.[8].

II. PRELIMINARIES

A. Basic Adders:

Half adder, full adders are the basic building blocks while performing addition, subtraction, multiplication and division. Half adder requires one XOR gate and one AND gate . By using AOI technology [9]-[10] theoretical gate count can be computed as follows.

$$\text{Gate count} = 6(1\text{XOR} + 1\text{AND}) \rightarrow (1)$$

Half adder consumes three units of delay for generation of sum and one unit of delay for generation of carry.

Full adder requires two Half adders and OR gate for generation of sum and carry. By using AOI technology the gate count for full adder can be computed as follows.

$$\text{Gate count} = 13(2\text{ HA} + 1\text{ OR gate}) \rightarrow (2)$$

Full adder consumes six units of delay for generation of sum and five units of delay for generation of carry.

B. 4bit Ripple Carry Adder:

A 4 Bit Ripple Carry Adder is designed by using Half adder and three Full adders.

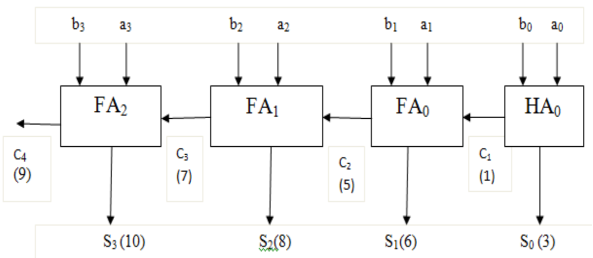

Fig.1 Ripple Carry Adder (4 bit) with input carry=0

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 10, October 2016

1) The inputs for HA are a_0, b_o and outputs are s_o, c_1. Generation of s_0 requires three units of delay and carry c_1 requires one unit of delay.
2) The inputs for FA_0 are a_1, b_1 and outputs are s_1, c_2. Generation of s_1 requires six units of delay and carry c_2 requires five units of delay.
3) The inputs for FA_1 are a_2, b_2 and outputs are s_2, c_3. Generation of s_2 requires Eight units of delay and carry c_3 requires seven units of delay.
4) The inputs for FA_2 are a_3, b_3 and outputs are s_3, c_4. Generation of s_3 requires ten units of delay and carry c_4 requires nine units of delay.

The delay evaluation methodology for each adder is explained as follows.

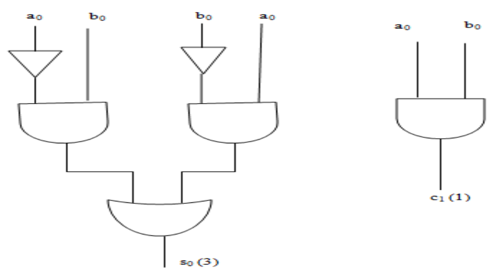

Fig.2 Delay evaluation Methodology for HA_0

The inputs for HA_0 are $b_{0,}$ a_0 and outputs are $s_0(3)$, $c_0(1)$. Generation of $s_0(3)$ requires three units of delay and carry $c_0(1)$ requires one unit of delay.

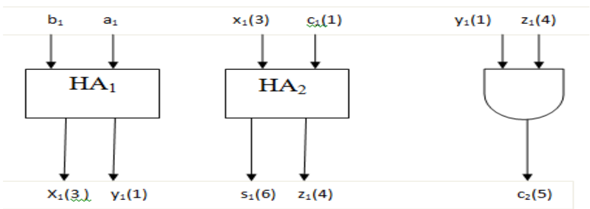

Fig.3 Delay evaluation Methodology for FA_0

The inputs for HA_1 are $b_{1,}$ a_1 and outputs are $X_1(3)$, $y_1(1)$ Generation of $X_1(3)$ requires three units of delay and carry $y_1(1)$ requires one unit of delay.
The inputs for HA_2 are $X_1(3)$, $C_1(1)$ and outputs are $s_1(6)$ $z_1(4)$. Generation of $s_1(6)$ requires six units of delay and carry $z_1(4)$ requires four units of delay.
The inputs for AND are $y_1(1)$, $z_1(4)$ and output is $c_2(5)$. Generation of $c_2(5)$ requires five units of delay.

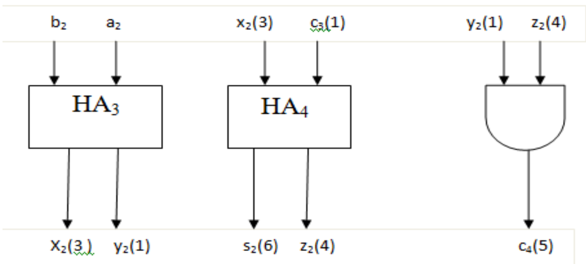

Fig.4 Delay evaluation Methodology for FA_1

The inputs for HA_3 are b_2 a2 and outputs are $X_2(3)$, $y_2(1)$. Generation of $X_2(3)$ requires three units of delay and carry $y_2(1)$ requires one unit of delay.
The inputs for HA_4 are $X_2(3)$, $C_2(1)$ and outputs are $s_2(6)$, $z_2(4)$. Generation of $s_2(6)$ requires six units of delay and carry $z_2(4)$ requires four units of delay.
The inputs for AND are $y_2(1)$, $z_2(4)$ and output is $c_4(5)$. Generation of $c_4(5)$ requires five units of delay.

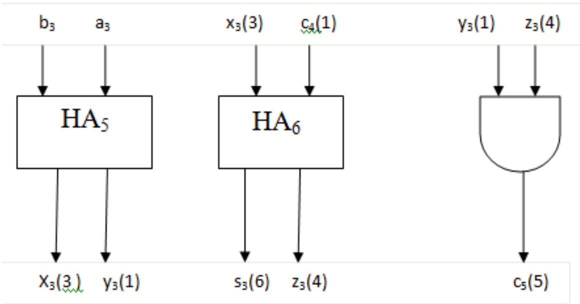

Fig.5 Delay evaluation Methodology for FA_2

The inputs for HA_5 are b_3, a3 and outputs are $X_3(3)$, $y_3(1)$. Generation of $X_3(3)$ requires three units of delay and carry $y_3(1)$ requires one unit of delay.
The inputs for HA_6 are $X_3(3)$, $C_3(1)$ and outputs are $s_3(6)$, $z_3(4)$. Generation of $s_3(6)$ requires six units of delay and carry $z_3(1)$ requires four units of delay.
The inputs for AND are $y_3(1)$, $z_3(4)$ and output is $c_5(5)$. Generation of $c_5(5)$ requires five units of delay.

C. 4 Bit Carry Selective Adder

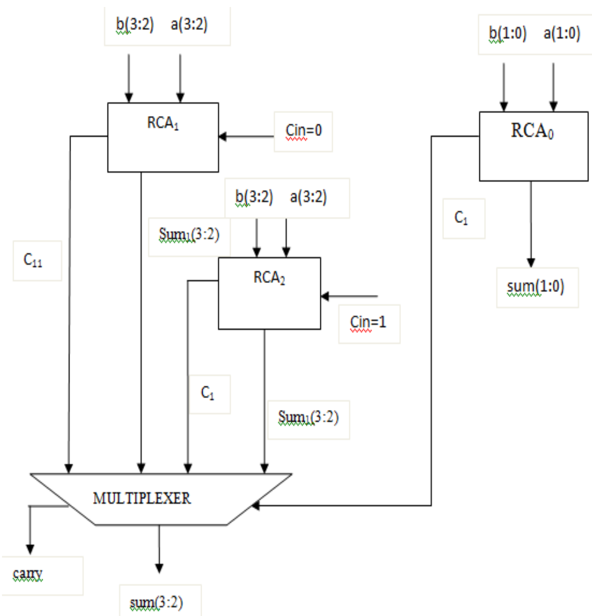

Fig.6 Carry selective adder(4 Bit)

The inputs for RCA_0 are b(1:0) a(1:0) and outputs are sum(1:0), $C_2(1)$. RCA_0 consists of two full adders. For first full adder the inputs are a(0),b(0),c_in and outputs are sum(0),$C_o(0)$.For second full adder the inputs are a(1),b(1), $C_o(0)$. and outputs are sum(1),$C_0(1)$.

DOI10.17148/IJARCCE.2016.51074

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 10, October 2016

The inputs for RCA_1 are b(3:2), a(3:2) ,Cin=0 and outputs are $s_2(3)$, $C_2(1)$. RCA_1 consists of two full adders. For first full adder the inputs are a(2),b(2),1'bo and outputs are sum(2),C1(2).For second full adder the inputs are a(3)b(3), $C_1(2)$. and outputs are sum(3),$C_{1(}3)$.
The inputs for RCA_2 are b(3:2), a(3:2) Cin=1 and output is $s_3(3)$, $C_3(1)$.

RCA_2 consists of two full adders. For first full adder the inputs are a(2),b(2), 1'b1 and outputs are sum_{11} (2),$C_{11}(2)$. For second full adder the inputs are a(3),b(3), $C_{11}(2)$. and outputs are sum $_{11}(3)$,C $_{11}(3)$.

The inputs for multiplexer are $sum_1(2)$, $sum_1(3)$, $sum_{11}(2)$, $sum_{11}(3)$, c_1, c_{11} and selection line is c1. Outputs are sum(2), sum(3) & carry.

It consists three ripple carry adders and three multiplexers.

RCA_0
Generation of sum(0) requires Six units of delay and carry $C_o(0)$ requires five units of delay.
Generation of sum(1) requires eight units of delay and carry $C_0(1)$ requires seven units of delay.

RCA_1
Generation of sum_1 (2) requires Six units of delay and carry $C_1(2)$ requires five units of delay.
Generation of sum $_1(3)$ requires eight units of delay and carry $C_1(3)$ requires seven units of delay.

RCA_2
Generation of sum_{11} (2) requires Six units of delay and carry C $_{11}(2)$ requires five units of delay.
Generation of sum_{11} (3) requires eight units of delay and carry C $_{11}(3)$ requires seven units of delay.
For the first multiplexer the inputs are sum_1 (2), sum_{11} (2), $C_0(1)$ and output is sum(2). Generation of sum (2) requires ten units of delay.

For the second multiplexer the inputs are sum $_1(3)$,sum_{11} (3) , $C_0(1)$ and output is sum(3). Generation of sum (3) requires ten units of delay.

For the third multiplexer the inputs are $C_1(3)$, $C_{11}(3)$, $C_0(1)$ and output is C_out .Generation of C_out requires seven units of delay.

Area evaluation methodology for CSLA:
Rca0 having two Full adders. Hence its gate count is 2x13=26
Rca1 having two Full adders. Hence its gate count is 2x13=26
Rca2 having two Full adders. Hence its gate count is 2x13=26
Three multiplexers having gate count is 3x4=12
Total gate count is 90.

Area evaluation methodology for 4 bit CSLA adder:

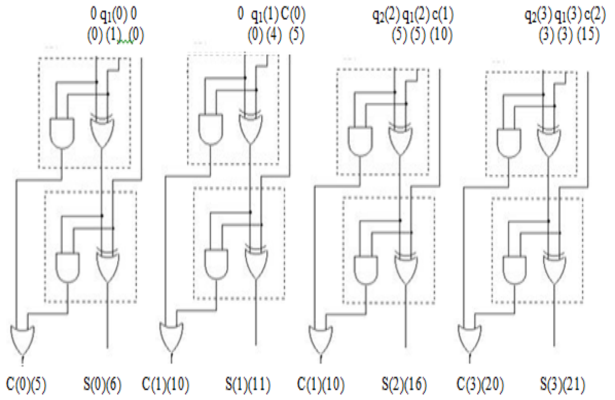

Fig 7. Delay evaluation for intermediate signal generation

The above diagram generates c(0), s(0) which has delay of 5& 6 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.
The above diagram generates c(1), s(1) which has delay of 10& 11 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.
The above diagram generates c(2), s(2) which has delay of 10& 16 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.
The above diagram generates c(3), s(3) which has delay of 20 & 21 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.

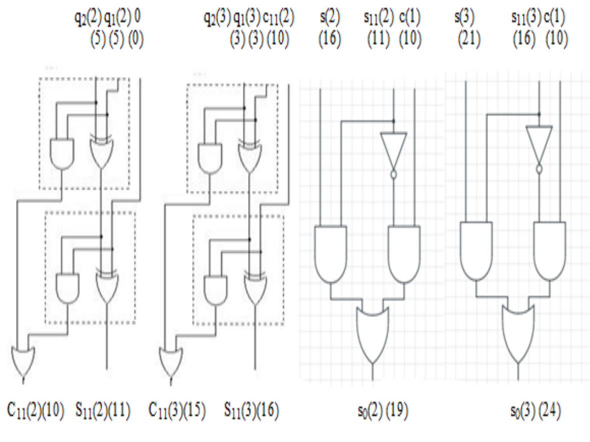

Fig. 8 Delay evaluation for intermediate signal generation

The above diagram generates $c_{11}(2)$, $s_{11}(2)$ which has delay of 10 &11 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.
The above diagram generates $c_{11}(3)$, $s_{11}(3)$ which has delay of 15& 16 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.
The above diagram generates $s_0(2)$ which has delay of 19 respectively. For this it requires one NOT gate, two AND gates & one OR gate.
The above diagram generates $s_0(3)$ which has delay of 24 respectively. For this it requires one NOT gate, two AND gates & one OR gate.

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 10, October 2016

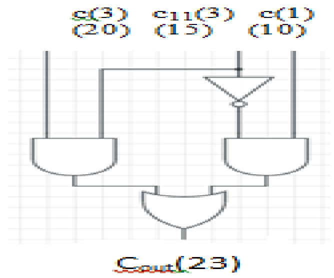

Fig.9 Delay evaluation for intermediate signal generation

The above diagram generates C_{out} which has delay of 23 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.

Area evaluation methodology for 6 bit CSLA adder (Z_7):

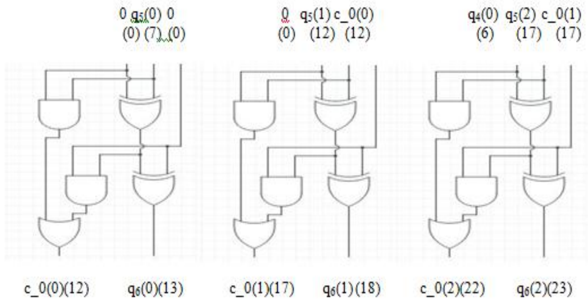

Fig. 10 Delay evaluation for intermediate signal generation

The above diagram generates c_0(0), $q_6(0)$ which has delay of 12&13 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.
The above diagram generates c_0(1), $q_6(1)$ which has delay of 17& 18 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.
The above diagram generates c_0(2), $q_6(2)$ which has delay of 22 & 23 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.

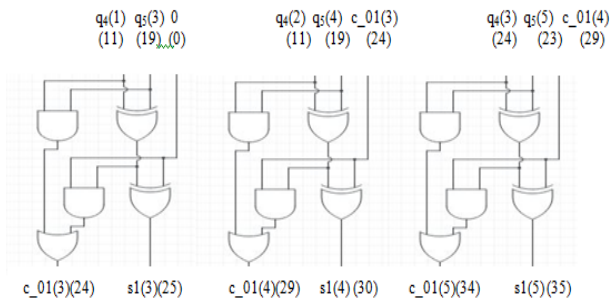

Fig.11 Delay evaluation for intermediate signal generation

The above diagram generates c_01(3), s_01(3) which has delay of 24&25 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.
.The above diagram generates c_01(4), s_01(4) which has delay of 29& 30 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.

The above diagram generates c_01(5), s_01(5) which has delay of 34&35 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.

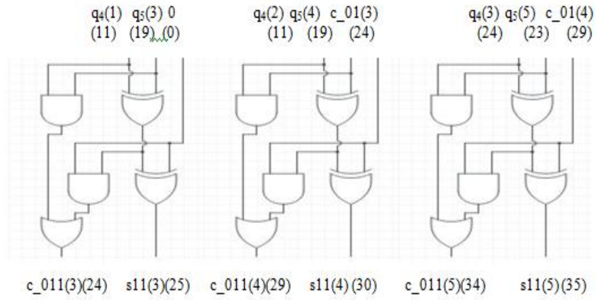

Fig. 12 Delay evaluation for intermediate signal generation

The above diagram generates c_011(3), s11(3) which has delay of 24&25 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.
The above diagram generates c_011(4), s11(4) which has delay of 29& 30 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.
The above diagram generates c_011(5), s11(5) which has delay of 34&35 respectively. For this it requires two Ex-OR gates, two AND gates & one OR gate.

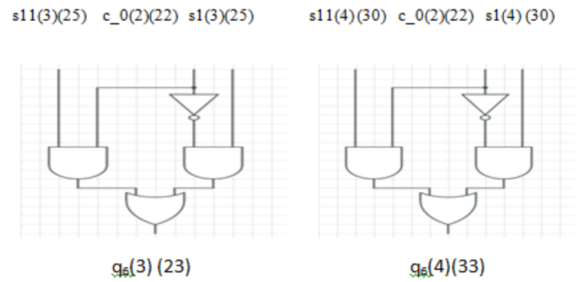

Fig.13 Delay evaluation for intermediate signal generation

The above diagram generates $q_6(3)$ which has delay of 23 respectively. For this it requires one NOT gate, two AND gates & one OR gate.

The above diagram generates $q_6(4)$ which has delay of 33 respectively. For this it requires one NOT gate, two AND gates & one OR gate.

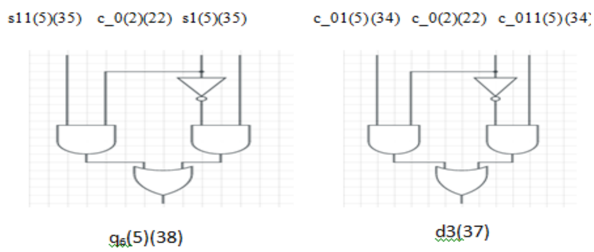

Fig. 14 Delay evaluation for intermediate signal generation

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319 5940
International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 10, October 2016

The above diagram generates $q_6(5)$ which has delay of 38 respectively. For this it requires one NOT gate, two AND gates & one OR gate.
The above diagram generates d_3 which has delay of 37 respectively. For this it requires one NOT gate, two AND gates & one OR gate.

III VEDIC MULTIPLIER USING 4 BIT KOGGSTONE ADDER

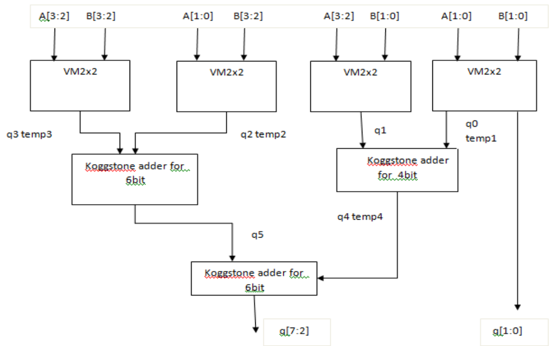

Fig.15 Vedic Multiplier using 4 Bit Koggstone adder

It consists of four 2x2 Vedic multiplier modules.
The inputs for first VM 2x2 module are A(1:0), B(1:0) and outputs are qo(temp1), q(1:0).
The inputs for second VM 2x2 module are A(3:2), B(1:0) and output is q1.
The inputs for third VM 2x2 module are A(1:0), B(3:2) and output is q2(temp2).
The inputs for fourth VM 2x2 module are A(3:2), B(3:2) and output is q3(temp3).
The inputs for 6Bit KSA are q3(temp3), q2(temp2) and output is q5(temp5).
The inputs for 4 Bit KSA are q0(temp1), q1 and output is q4.
The inputs for 6Bit KSA are q5(temp5), q4(temp4) and output is q(7:2).

$g_0 = a_o$ and b_o →(3)
$p_0 = a_o$ xor b_o-→ (4)
$c_1 = g_o + p_o c_{in}$-→(5)
$c_2 = g_1 + p_1 g_o + p_1 p_o c_{in}$ →(6)
$c_3 = g_2 + p_2 g_o + p_2 p_1 c_1$→(7)
$c_2 = g_3 + p_3 g_2 + p_3 p_2 (g_1 + p_1 g_o) + p_3 p_2 p_1 p_o c_{in}$ -→(8) [11]-[12].

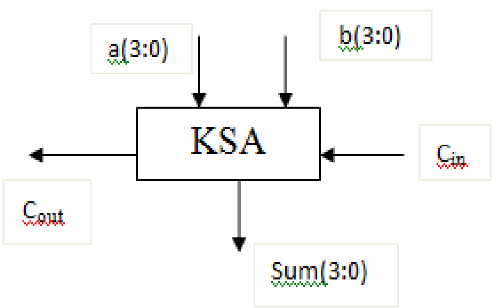

Fig 16 KSA adder (4 bit)

Delay evaluation for 4bit KSA:
It consists eight XOR gates and thirteen AND gates and finally it also consists four OR gates.

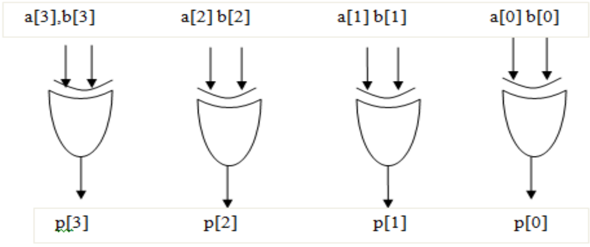

Fig.17 Delay evaluation Methodology for first four XOR gates

For first XOR gate, the inputs are a(0),b(0)and output is p(0), Generation of p(0) requires three units of delay.
For second XOR gate, the inputs are a(1),b(1)and output is p(1), Generation of p(1) requires three units of delay.
For third XOR gate, the inputs are a(2),b(2)and output is p(2), Generation of p(2) requires three units of delay.
For fourth XOR gate, the inputs are a(3),b(3)and output is p(3), Generation of p(3) requires three units of delay.

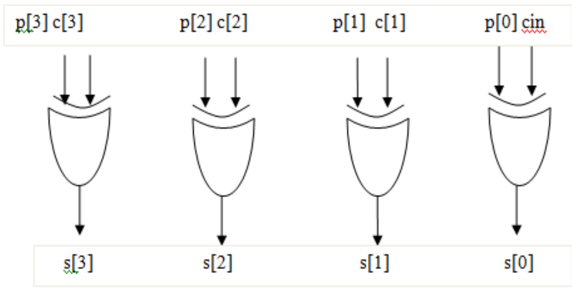

Fig.18 Delay evaluation Methodology for next four XOR gates

For fifth XOR gate, the inputs are Cin, p(0)and output is Cin, Generation of s(0) requires six units of delay.
For six XOR gate, the inputs are c(1),p(1)and output is s(1), Generation of s(1) requires eight units of delay.
For seven XOR gate, the inputs are c(2),p(2)and output is s(2), Generation of s(2) requires eight units of delay.
For eighth XOR gate, the inputs are c(3),p(3)and output is s(3), Generation of s(3) requires ten units of delay.

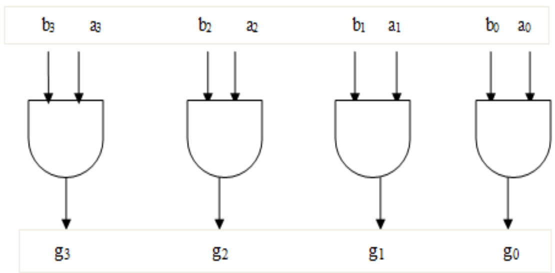

Fig.19 Delay evaluation Methodology for first four AND gates

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 10, October 2016

For first AND gate, the inputs are a(0),b(0)and output is g(0), Generation of g(0) requires one unit of delay.
For second AND gate, the inputs are a(1),b(1)and output is g(1), Generation of g(1) requires one unit of delay.
For third AND gate, the inputs are a(2),b(2)and output is g(2), Generation of g(2) requires one unit of delay.
For fourth AND gate, the inputs are a(3),b(3)and output is g(3), Generation of g(3) requires one unit of delay.

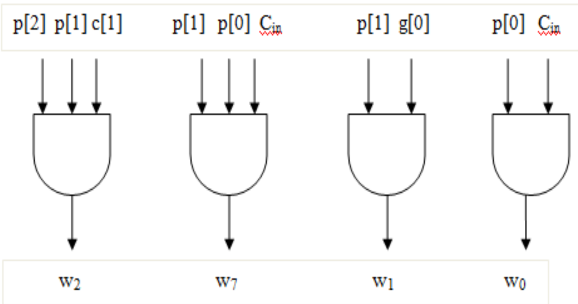

Fig.20 Delay evaluation Methodology for next four AND gates

For fifth AND gate, the inputs are p(0),Cin and output is w(0), Generation of w(0) requires four units of delay.
For sixth AND gate, the inputs are p(1),g(0)and output is w(1), Generation of w(1) requires four unit s of delay.
For seventh AND gate, the inputs are p(1),p(0),Cin and output is w(7), Generation of w(7) requires four units of delay.
For eighth AND gate, the inputs are p(2), p(1), Cin and output is w(2), Generation of w(2) requires six units of delay.

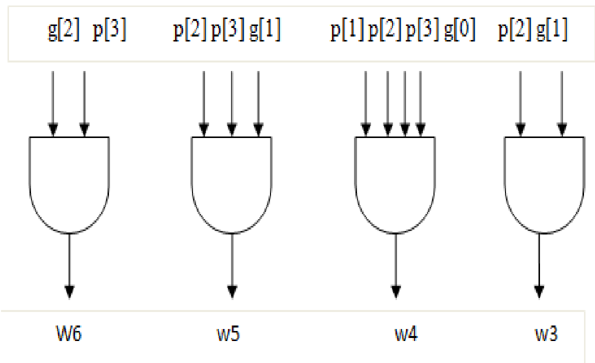

Fig.21 Delay evaluation Methodology for next four AND gates

For ninth AND gate, the inputs are p(2),g(1))and output is w(3), Generation of w(3) requires four units of delay.
For tenth AND gate, the inputs are p(2), p(1), p(3),g(0)and output is w(4), Generation of w(4) requires four units of delay.
For eleventh AND gate, the inputs are p(2),p(3),g(1) and output is w(5), Generation of w(5) requires four units of delay.
For twelfth AND gate, the inputs are g(2),p(3),and output is w(6), Generation of w(6) requires four units of delay.

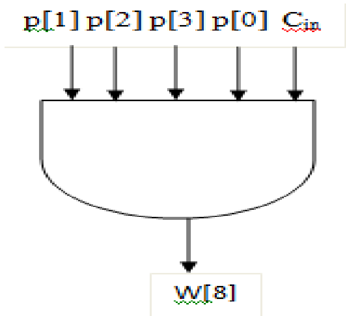

Fig.22 Delay evaluation Methodology for intermediate signal generation

For thirteenth AND gate, the inputs are p(1),p(0), p(2),p(3),Cin and output is w(8), Generation of w(8) requires four units of delay.

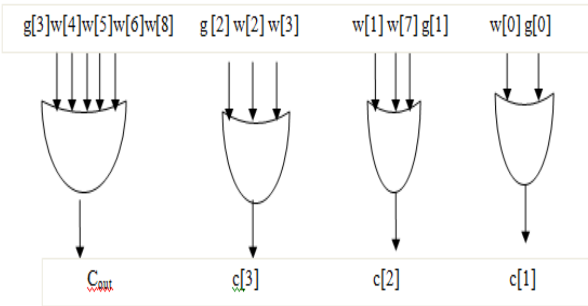

Fig.23 Delay evaluation Methodology for four OR gates

For first OR gate, the inputs are w(0),g(0)and output is c(1), Generation of c(1) requires five units of delay.
For second OR gate, the inputs are w(1), g(1) , w(7) and output is c(2), Generation of c(2) requires five units of delay.
For third OR gate, the inputs are w(2),w(3), g(2) and output is c(3), Generation of c(3) requires five units of delay.
For fourth OR gate, the inputs are w(4),w(5), w(6) w(8),g(3)and output is Cout, Generation of Cout requires five units of delay.
Gate Count: It consists eight XOR gates hence its gate count is 8x5=40 It consists thirteen AND gates hence its gate count is 13x1=13 also consists four OR gates hence its gate count is 4x1=4 Total gate count is 57.

Delay evaluation for 6bit KSA:
Generation of propagation signals p(0), p(1), p(2), p(3) , p(4), p(5) requires three units of delay.
For seventh XOR gate, the inputs are Cin, p(0)and output is Cin, Generation of s(0) requires six units of delay.
For eighth XOR gate, the inputs are c(1),p(1)and output is s(1), Generation of s(1) requires eight units of delay.
For ninth XOR gate, the inputs are c(2),p(2)and output is s(2), Generation of s(2) requires eight units of delay.
For tenth XOR gate, the inputs are c(3),p(3)and output is s(3), Generation of s(3) requires ten units of delay.
For eleventh XOR gate, the inputs are c(4),p(4)and output is s(4), Generation of s(4) requires eight units of delay.

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 10, October 2016

For twelfth XOR gate, the inputs are c(5),p(5)and output is s(5), Generation of s(5) requires ten units of delay.
For generate signals g(0), g(1), g(2), g(3), g(4), g(5) requires one uint of delay.
For seveth AND gate, the inputs are p(0),Cin and output is w(0), Generation of w(0) requires four units of delay.
For eighth AND gate, the inputs are p(1),g(0)and output is w(1), Generation of w(1) requires four unit s of delay.
For ninth AND gate, the inputs are p(1),p(0),Cin and output is w(7), Generation of w(7) requires four units of delay.
For tenth AND gate, the inputs are p(2), p(1), Cin and output is w(2), Generation of w(2) requires six units of delay.

For eleventh AND gate, the inputs are p(2),g(1))and output is w(3), Generation of w(3) requires four units of delay.
For twelfth AND gate, the inputs are p(2), p(1), p(3),g(0)and output is w(4), Generation of w(4) requires four units of delay.
For thirteenth AND gate, the inputs are p(2),p(3),g(1) and output is w(5), Generation of w(5) requires four units of delay.
For fourteenth AND gate, the inputs are g(2),p(3),and output is w(6), Generation of w(6) requires four units of delay.
For fifteenth AND gate, the inputs are p(1),p(0), p(2),p(3),Cin and output is w(8), Generation of w(8) requires four units of delay.
For sixteenth AND gate, the inputs are p(4),g(3)and output is w(9), Generation of w(9) requires one unit of delay.
For seventeenth AND gate, the inputs are p(4),p(3),g(2) and output is w(10), Generation of w(10) requires one unit of delay.

For eighteenth AND gate, the inputs are p(2), p(4), p(3),g(1)and output is w(11), Generation of w(11) requires four units of delay.
For nineteenth AND gate, the inputs are p(2), p(4), p(3),c(1), p(1), and output is w(12), Generation of w(12) requires four units of delay.
For twentieth AND gate, the inputs are p(5),g(4)and output is w(13), Generation of w(13) requires four units of delay.
For twenty first AND gate, the inputs are p(5), p(4), g(3), and output is w(14), Generation of w(14) requires four units of delay.
For twenty second AND gate, the inputs are p(4), p(5), p(3),g(2)and output is w(15), Generation of w(15) requires four units of delay.
For twenty third AND gate, the inputs are p(5), p(4), p(3),p(2,c(2) and output is w(16), Generation of w(16) requires six units of delay.
For first OR gate, the inputs are w(0),g(0)and output is c(1), Generation of c(1) requires five units of delay.
For second OR gate, the inputs are w(1), g(1) , w(7) and output is c(2), Generation of c(2) requires five units of delay.

For third OR gate, the inputs are w(2),w(3), g(2) and output is c(3), Generation of c(3) requires five units of delay.
For fourth OR gate, the inputs are w(4),w(5), w(6) w(8),g(3)and output is C(4) Generation of C(4) requires five units of delay.
For fifth OR gate, the inputs are w(12), w(11) w(10),w(9), g(4)and output is C(5) Generation of C(5) requires five units of delay.
For fifth OR gate, the inputs are w(13), w(14) w(15),w(16), g(5)and output is C_{out} Generation of C_{out} requires seven units of delay.
Gate Count:
It consists twelve XOR gates hence its gate count is 12x5=60 and twenty three AND gates hence its gate count is 23x1=23 and finally it also consists six OR gates hence its gate count is 6x1=6 Total gate count is 89.
Delay evaluation methodology for 4 bit KSA adder:

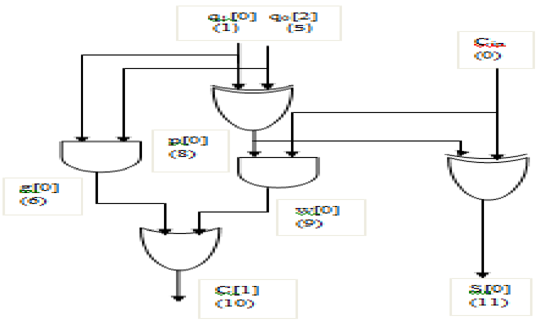

Fig.24 Delay evaluation Methodology for intermediate signal generation

The diagram in the above figure 24 gives s(0) and c(1) which has delays 11 and 10 respectively . for generating s(0) and c(1) requires two XOR gates ,two AND gates and one OR gate.

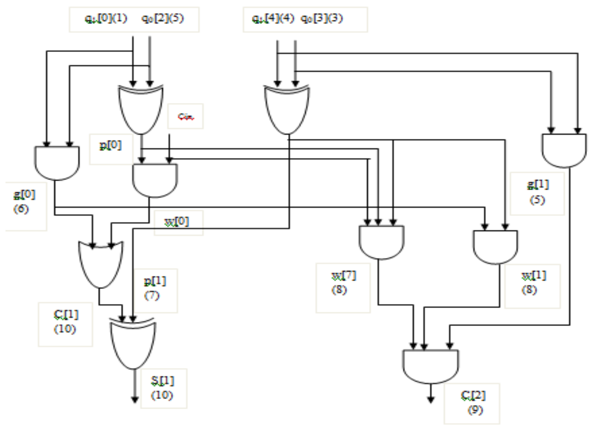

Fig.25 Delay evaluation Methodology for intermediate signal generation

The diagram in the above figure 25 gives s(1) and c(2) which has delays 10 and 9 respectively . for generating s(1) and c(2) requires three XOR gates , six AND gates and one OR gate.

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 10, October 2016

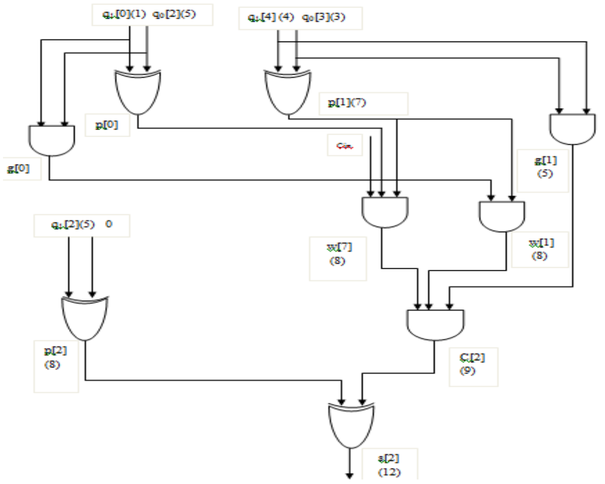

Fig.26 Delay evaluation Methodology for intermediate signal generation

The diagram in the above figure 26 gives s(2) which has delays 12 . For generating s(2) requires four XOR gates and five AND gates.

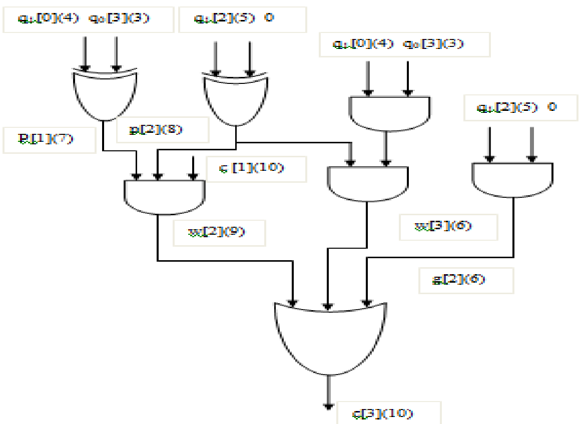

Fig.27 Delay evaluation Methodology for intermediate signal generation

The diagram in the above figure 27 givesc(3) which has delays 10. For generating c(3) requires two XOR gates , four AND gates and one OR gate.

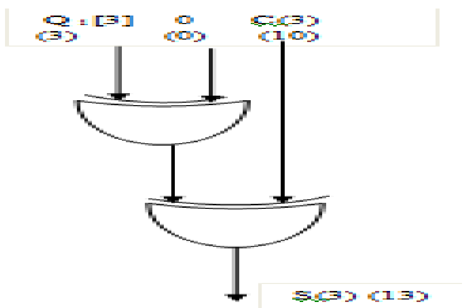

Fig..28 Delay evaluations Methodology for intermediate signal generation

The diagram in the above figure 28 gives s(3) which has delays 13 . for generating s(3) requires two XOR gates.

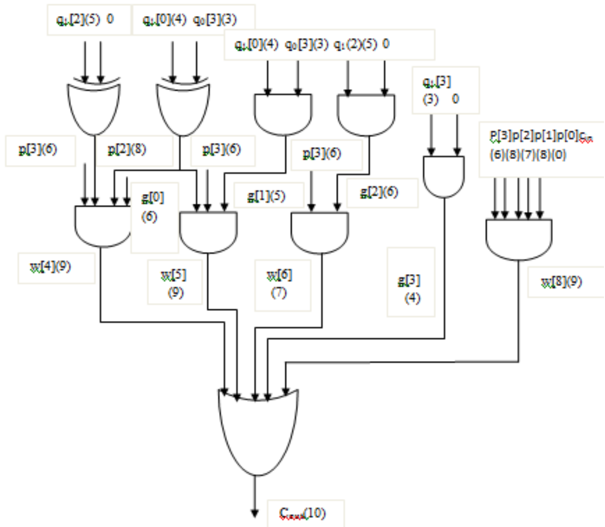

Fig. 29 Delay evaluation Methodology for intermediate signal generation

The diagram in the above figure 29 gives c_{out} which has delays 10. For generating c_{out} requires two XOR gates , seven AND gates and one OR gate.

Delay evaluation methodology for 6 bit KSA adder:

.

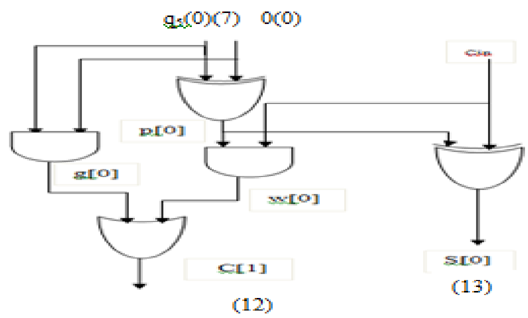

Fig. 30 Delay evaluation Methodology for intermediate signal generation

The diagram in the above figure 30 gives s(0) and c(1) which has delays 13 and 12 respectively . for generating s(1) and c(2) requires two XOR gates , two AND gates and one OR gate.

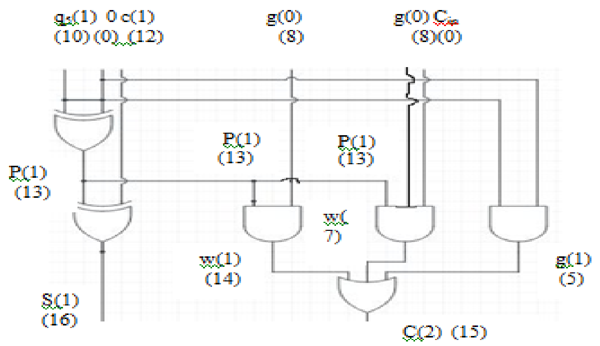

Fig.31 Delay evaluation Methodology for intermediate signal generation

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 10, October 2016

The diagram in the above figure 31 gives s(1) and c(2) which has delays 16 and 15 respectively . for generating s(1) and c(2) requires three XOR gates , six AND gates and one OR gate.

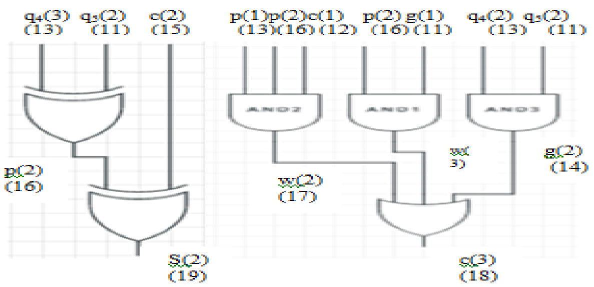

Fig. 32 Delay evaluation Methodology for intermediate signal generation

The diagram in the above figure 32 gives s(2) and c(3) which has delays 19 and 18 respectively . for generating s(2) and c(3) requires two XOR gates , three AND gates and one OR gate.

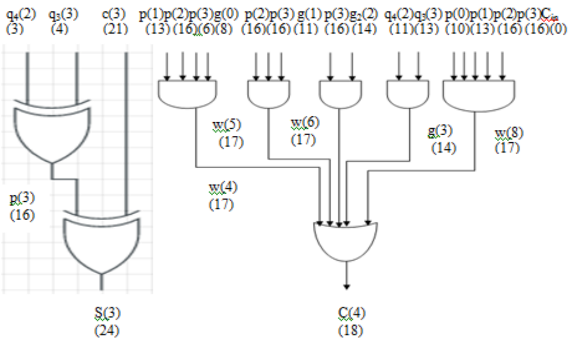

Fig. 33 Delay evaluation Methodology for intermediate signal generation

The diagram in the above figure 33 gives s(3) and c(4) which has delays 24 and 18 respectively . for generating s(3) and c(4) requires two XOR gates , five AND gates and one OR gate.

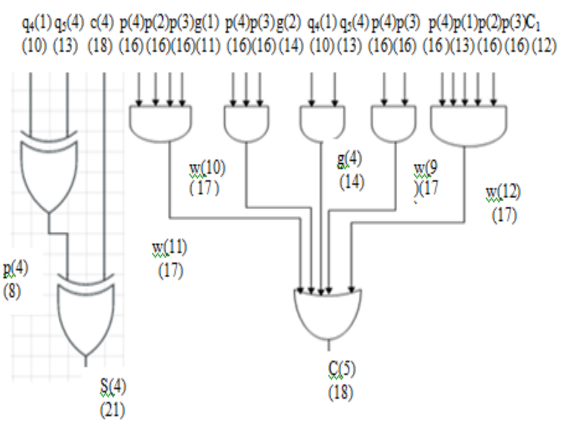

Fig.34 Delay evaluation Methodology for intermediate signal generation

The diagram in the above figure 34 gives s(4) and c(5) which has delays 21 and 18 respectively . for generating s(4) and c(5) requires two XOR gates , five AND gates and one OR gate.

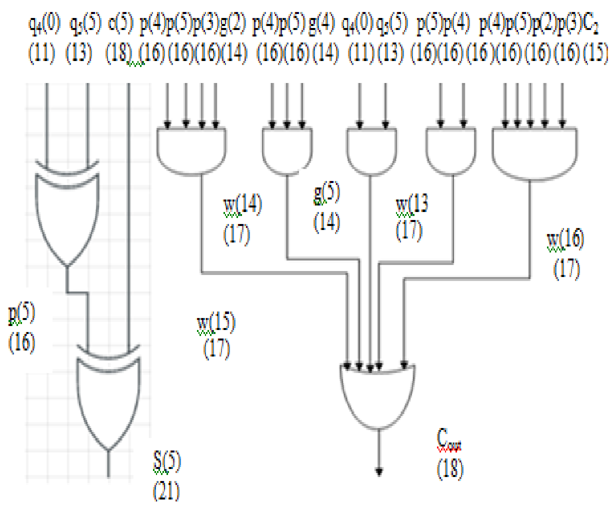

Fig. 35 Delay evaluation Methodology for intermediate signal generation

The diagram in the above figure 35 gives s(5) and c_{out} which has delays 21 and 18 respectively . for generating s(5) and c_{out} requires two XOR gates , five AND gates and one OR gate.

Table 1 gives Theoretical area evaluation methodology for basic multiplier blocks.

Table 1 Theoretical Area Evaluation

Vedic Module	VM with normal adders	VM with BEC adders	VM with CSLA adders	VM with Koggstone adders
4x4	257	390	393	305

Theoretical delay evaluation methodology for Vedic multipliers (4 Bit) using CSLA and KSA adders is carried out. Delay values are represented in table 2.

Table 2 Theoretical Delay Evaluation

	q_0 (0)	q_0 (1)	q_6 (0)	q_6 (1)	q_6 (2)	q_6 (3)	q_6 (4)	q_6 (5)	Cout
CSLA	1	4	13	18	23	28	33	38	37
KSA	1	4	13	16	19	24	19	19	18

IV. SIMULATION RESULTS

The proposed architecture is implemented using Xilinx ISIM tool for simulation on a INTEL core2 (TM) Duo processor, 32 bit operating System, RAM 2 GB with 2.93GHZ clock frequency. Initially two 4 bit inputs are taken into consideration & the results are presented. Carry Select Adder, ripple carry adder, koggstone adder for 4 bit, 8 bit; 16 bit Vedic multipliers are simulated on Xilinx ISE 12.2. The Input output waveforms which are generated by using XILINX software are shown in below figure 36.

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 10, October 2016

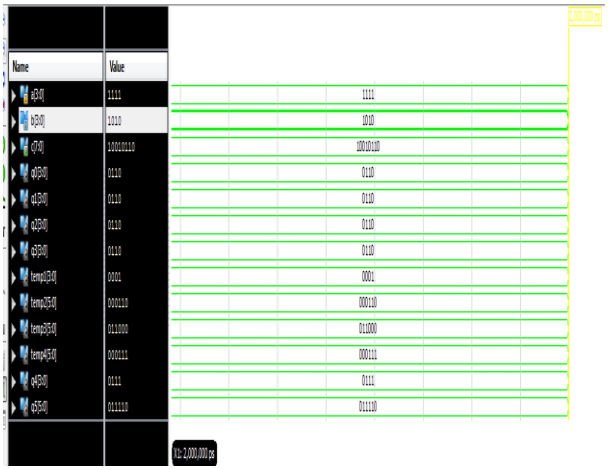

Fig. 36 Simulation Results for 4 bit vedic multiplier using KSA adders

The inputs for KSA a(3:0) ,b(3:0) ,Cin for 4 bit are taken as a "1111", "1010", '1' and the obtained output is "10010110".After Simulation HDL Synthesis is performed.

Performance analysis for Vedic multiplier using KSA &CSLA shown in Table 3

Table 3 Practical power evaluation

Supply power(mW)	Dynamic power	Quiescent power	Total power
KSA	1.98	81.01	82.99
CSLA	2.13	81.01	83.14

It is observed that KSA architecture is consuming less power when compared to CSLA architecture. This is shown in fig. 37

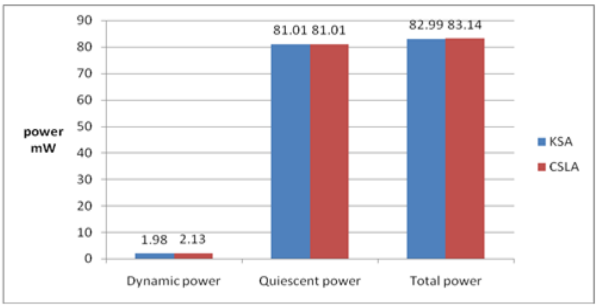

Fig 37. Graphical representation of power comparision of Vedic multiplier using KSA & CSLA.

Table 4 Memory comparison of Vedic Multipliers using KSA and CSLA adders

	Memory (synthesis Report) KB	Memory (Translation Report) KB
KSA	189384	140132
CSLA	189384	128932

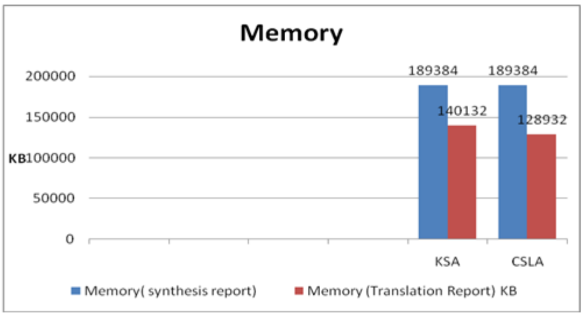

Fig. 38 Comparison of memory utilized for Vedic Multiplier using KSA and CSLA

It is observed that CSLA architectures are having less memory when compared to KSA architectures. This result is shown in fig 38.

V. CONCLUSION

Vedic Multipliers using KSA and CSLA architectures are implemented. A comparison is made between these two architectures with respect to power consumption and memory occupation. It can be concluded that CSLA architecture is better than KSA architecture.

REFERENCES

[1] Aravind E Vijayan, A. John and D. Sen, "Efficient Implementation of 8-bit Vedic Multipliers for Image Processing Application", International Conference on Contemporary Computing and Informatics [IC3I], 2014.

[2]. G.Vaithiyanathan, K.Venkatesan, S.Sivaramakrishnan, S.Siva, and S.Jayakumar, "Simulation and Implementation of Vedic Multiplier Using VHDL Code" International Journal of Scientific & Engineering Research Volume 4, Issue 1, January-2013.

[3]. Y.RamaLakshmanna, Prof. G.V.S.Padma Rao, Prof. N.Udaya Kumar, K.Bala Sinduri et.al "A Survey on Different MultiplierTechniques "SSRG International Journal of Electronics and Communication Engineering[SSRG-IJECE]– Volume 3 Issue 3–March 2016 ISSN: 2348–8352 www.internationaljournalssrg.org Page 8

[4] V.Priyanka Brahmaiah ,L.Dhrma Teja, Dr Y.Padma sai "Study on comparison of various multipliers" International Journal of Electronics and communication engineering & technology [IJECET], ISSN 0976-6464 volume 4 Issue 5 September – October, 2013 pp-132-142.

[5] Ruchi Sharma "Analysis of Different Multiplier with Digital Filters Using VHDL Language" International Journal of Engineering and Advanced Technology [IJEAT] ISSN: 2249 – 8958, Volume-2, Issue-1, October 2012

[6] S.dhivya, Mr.T.Nallusamy "radix-8 modified booth recoder for high speed add-multiply operator" international conference on engineering trends and science & humanities [icetsh-2015] issn: 2348 – 8549 www.internationaljournalssrg.org page 1

[7] Sulakshna Thakur#1, Pardeep Kumar"Area-Efficient & High Speed Ripple Carry based Vedic Multiplier" SSRG International Journal of Electronics and Communication Engineering [SSRG-IJECE] – EFES April 2015 ISSN: 2348 - 8549 http://www.internationaljournalssrg.org Page 6

[8] Premananda B.S. Samarth S. Pai Sashank B Sashank S Bhat " Design and Implementation of 8 –bit Vedic multiplier" International Journal of Advanced research in Electrical, Electronics and Instrumentation Engineering[IJAREEIE] Vol. 2 Issue 12, December 2013 ISSN [online] 2278-8875

[9] B. Ramkumar, H.M. Kittur, and P. M.Kannan, "ASIC implementation of modified faster carry save adder," Eur. J.Sci. Res., vol. 42, no. 1, pp.53–58, 2010

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 10, October 2016

[10] Bala Sindhuri Kandula, K. Padma Vasavi, I. Santi Prabha"Area Efficient VLSI Architecture for Square Root Carry Select Adder Using Zero Finding Logic" Original Research Article Procedia Computer Science, Volume 89, 2016, Pages 640-650

[11].Sajesh Kumar, U,MohamedSalih K.K and Sajith K. "Design and Implementation of Carry Select Adder with out using Multiplexers"978-4673-1627- 9112/$31.00 2012 IEEE.

[12] B.Tapasvi ,G.S.S.B.Lakshmi ,K.Bala Sinduri, N. Udaya Kumar "Implementation of 64-Bit Kogge Stone Carry Select Adder with ZFC for Efficient Area " 978-1-4799-6085-9/15/$31.00 ©2015 IEEE

BIOGRAPHIES

Rama Lakshmanna Y received his B.E. Degree in Electronics & communication ngineering from S.R.K.R Engineering College, Bhimavaram and M.Tech degree in Computer Science Engineering from Jawaharlal Nehru Technological University, Kakinada. At present he is working as Associate Professor at SRKR Engineering College, Bhimavaram. He has 16 years of teaching experience and guided many UG & PG projects. He has published 3 research papers in International Conferences He is a member of IETE and Fellow of IE. At present he is pursuing M.Tech degree in Communication System at SRKR Engineering College, Bhimavaram. His areas of interest are Very Large Scale Integrated Circuits and Communication Systems, and Digital Image Processing,

Padma Rao G.V.S. received his B.E Degree in Electronics & communication engineering from S.R.K.R Engineering College, Bhimavaram and M.Tech degree in Communication System from REC Kurukshetra. At present he is working as Professor at SRKR Engineering College, Bhimavaram. He has 20 years of teaching experience and guided many UG & PG projects. His areas of interest are Digital Image Processing, Digital Signal Processing and Very Large Scale Integrated Circuits. He has published 5 research papers in International and National Conferences He is a member of ISTE.

BalaSindhuri K received her B.E degree in Electronics & communication engineering from S.R.K.R Engineering College, Bhimavaram and M.Tech degree in VLSI System Design from Shri Vishnu Engineering College for women Vishnupur, Bhimavaram. At present, she is working as an Assistant Professor at SRKR Engineering College, Bhimavaram. She has 5 years of teaching experience. Her areas of interests are Very Large Scale Integrated Circuits, Signal Processing and Image processing. She has published 18 research papers in International and National Conferences.

Udaya Kumar N received his M.Tech degree in Microwave Electronics from University of Delhi South Campus and is pursuing Ph.D degree in DIP at Jawaharlal Nehru Technological University, Hyderabad. At present he is working as Professor at SRKR Engineering College, Bhimavaram. He has 23 years of teaching experience and guided many UG & PG projects. His areas of interest are Digital Image Processing, Digital Signal Processing and Very Large Scale Integrated Circuits. He has published more than 30 research papers in International and National Conferences. One of his papers has been published as a book chapter in the research book published by Springer. He also co-authored several text books for engineering and diploma students. He is a member of IEEE and Fellow of IETE